REMARKS

Claims 1-20 are pending. By this amendment, claims 8 and 10 are cancelled, and claims 1, 4, 11, 14, and 19 are amended. No new matter is introduced. Support for the amendments may be found at least at page 3, lines 11-13, page 8, line 31 to page 9, line 1, page 9, lines 3-10, page 9, lines 11-21, page 9, line 29, to page 10, line 4, page 12, line 30 to page 13, line 7 of the specification. Reconsideration and allowance of the claims in view of the above amendments and the remarks that follow are respectfully requested.

Claim Interpretation

On page 2 the Office Action "declares the claim feature of the clock signal active after each data input passes each latch as a design choice for the reason being that whether the signal arrives before or after the time interval relative to the clock is immaterial since the circuit may not function in either case." Applicants respectfully traverse. As described in the specification at page 9, lines 3-10 (shown below), whether a signal arrives before or after the time interval relative to the clock is important in the present application:

> The second characteristic to be extracted is an opening time, referred to as a valid time, associated with a dummy latch node attached to each output port. The dummy latch node may be controlled by a derived clock that has an opening edge offset with respect to the opening edge of a clock port. The derived clock typically becomes active at the time corresponding to the latest signal arrival from the clock port to the output port in the modeled circuit. The dummy latch node compares data signal arrival at the output port with the clock signal arrival of the latest clock at the output port. All paths arriving before the latest clock stop at the dummy latch node, i.e., the paths are not transparent and the clock signal goes to the output port instead. If the data signal arrives after the clock signal, the data signal propagates to the output port.
>
> Multiple paths may converge from multiple input ports to one output port, with each path controlled by a different clock. In the timing abstraction model, the dummy latch node enables comparison of the data signal with the latest clock signal. Accordingly, the data signal may be blocked if the signal arrives earlier than any of the clocks converging to the output port. Comparing the paths with the most critical clock significantly reduces the number of paths that arrive at the output port.

(Emphasis added). These features are recited in amended claims 1, 11, and 14. If the input signal arrives before the clock signal, the input signal cannot cause any violation in the design circuitry downstream from the echo circuit that would not be visible on the clock to output timing path. Therefore, it is not necessary to propagate the input signal to the output of the echo circuit. Conversely, if the input signal arrives after the clock signal, the input signal can

potentially cause a violation in the design circuitry downstream from the echo circuit that would not occur on the clock to output timing path. Therefore, it is necessary to propagate the input signal to the output of the echo circuit. The determination whether or not to propagate the input signal to the output port as function of the clock signal is not simply a design choice - it is a necessary feature to assure that all timing violations that would normally be detected in a design will also be detected when the modeled circuit block is represented by the echo circuit. Furthermore, the clock signal arrival is not a function of the input signal arrival but rather a reference dependent on clock pin arrival times and the delays in the modeled circuit.

Claim Rejections Under 35 U.S.C. §103

On page 3 the Office Action rejects claims 1-20 under 35 U.S.C. § 103(a) over U.S. Patent 6,453,436 to Rizzolo (hereafter Rizzolo) in view of U.S. Patent 6,023,568 to Segal (hereafter Segal) and further in view of U.S. Patent 6,158,022 to Avidan (hereafter Avidan). With respect to claim 1, the Office Action asserts that Segal teaches "wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a clock signal from a most critical clock element controlling the output port (design choice: see claim interpretation); identifying relevant timing paths in the echo-circuit, wherein the relevant timing paths are associated with the plurality of parameters (Segal: column 7, lines 4-25 and column 8, lines 18-36)." This rejection is respectfully traversed.

Claims 8 and 10 are cancelled, rendering the rejection of claims 8 and 10 moot.

To establish a *prima facie* case of obviousness ... the prior art reference (or references when combined) must teach or suggest all of the claim limitations. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and MPEP § 2142. If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and MPEP § 2143.03.

Segal is directed to a method for constructing a model of a digital circuit that contains level sensitive latches. The model allows for time borrowing amongst latches. Chains of latches or latch paths are collapsed together. The resulting model can be used for simulation or synthesis. Rizzolo is directed to a method and apparatus for improving transition fault testability of semiconductor chips. Avidan is directed to a circuit analyzer of black, gray and transparent elements. The circuit analyzer is adapted to run in the memory of a processing system and characterizes the performance of a circuit under test.

Segal is the primary reference cited in rejecting the claims. For transparent paths with more than two latches, Segal's abstraction model includes internal latch nodes on the input-to-output transparent paths (see the algorithm described in Figure 13a and 13b and in sections 4.3 and 4.4). Specifically, step 2140 in Figure 13b and the detailed description in section 4.4 explain that the routine recourses through individual levels of latches where the "startpoint" list for the next level constitutes latch fan-outs of a particular fan-out type from the previous level. Only the latches of the same fan-out type (controlled by the same clock) are collapsed at each latch level, but the number of latch levels remains the same. In other words, the input to output graph from Segal's model resembles a tree with the root at the input port. The number of levels of the tree corresponds to number of latches on input to output path and the number of latches at each level corresponds to the number of fan-out types at that level. Therefore, only the number of latches at each level is reduced with Segal's model, not the number of levels. Segal's model is not truly port-based.

Contrary to Segal, amended claim 1 recites: "the dummy latch node enables the signal to propagate from the input port to the output port only if the signal arrives at the output port later than a latest clock signal from any pin clock signal controlling the dummy latch node." Therefore, the echo-circuit (timing abstraction model) recited in amended claim 1 propagates to the output port only the signal path that arrives at the output port later than all clock-to-output paths, i.e., the most critical of all clock-to-output paths. In other words, the echo-circuit recited in claim 1 collapsed together and perform timing checks for all paths from a given input and for all paths to a given output. The level of abstraction in Segal's model is much less than the echo-circuit recited in amended claim 1.

Therefore, Segal does not disclose or suggest "wherein the echo-circuit is stimulus independent, port-based, has no internal latch nodes, and is used in any static timing analysis (STA) tools, wherein the echo-circuit includes a dummy latch node that is controlled by an internally generated clock signal that becomes active when a latest clock signal from the circuit arrives at the output port, and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a latest clock signal from any pin clock signal controlling the output port," as recited in amended claim 1.

Rizzolo and Avidan do not cure Segal's defect and do not disclose or suggest the above noted features. For example, Rizzolo's method pertains to design test. The method adds (as opposed to abstracting) to a circuit additional scan and multiplexor circuitry that will be implemented on a silicon die for verification of circuit functionality. Quite to the contrary,

the method recited in claim 1 creates an abstraction (echo circuit) of a real circuit for the purpose of simulating timing characteristics of this circuit through Static Timing Analysis. The echo circuit is not implemented on silicon die. Unlike the apparatus of Rizzolo, the method recited in claim 1 simplifies the circuit and abstracts away everything not necessary for timing simulation. In addition, Rizzolo's circuit is not port based - it contains an entire chain of scan latches between the scan input and scan input of the block. Since none of the references disclose or suggest all of the elements of amended claim 1, claim 1 is allowable.

Claims 2-7 and 9 are allowable at least because they depend from allowable claim 1 and for the additional features they recite.

Regarding claim 11, for the same reason as noted above with respect to claim 1, Segal, Rizzolo and Avidan, individually and in combination, do not disclose or suggest "wherein the echo-circuit is stimulus independent, port-based, has no internal latch nodes, and is used in any static timing analysis (STA) tools, wherein the echo-circuit includes a dummy latch node that is controlled by an internally generated clock signal that becomes active when a latest clock signal from the circuit arrives at the output port, and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a latest clock signal from any pin clock signal controlling the output port," as recited in amended claim 11. As noted above, the level of abstraction in Segal's model (the primary reference) is much less than the timing abstraction model recited in claim 11. Since the references do not disclose or suggest all elements of amended claim 11, claim 11 is allowable.

Claims 12-13 are allowable at least because they depend from allowable claim 11 and for the additional features they recite.

Regarding claim 14, for the same reason as noted above with respect to claim 1, Segal, Rizzolo and Avidan, individually and in combination, do not disclose or suggest "wherein the echo-circuit is stimulus independent, port-based, has no internal latch nodes, and is used in any static timing analysis (STA) tools, wherein the echo-circuit includes a dummy latch node that is controlled by an internally generated clock signal that becomes active when a latest clock signal from the circuit arrives at the output port, and wherein the echo-circuit enables a signal to propagate from an input port to an output port only if the signal arrives at the output port later than a latest clock signal from any pin clock signal controlling the output port," as recited in amended claim 14. As noted above, the level of abstraction in Segal's model (the primary reference) is much less than the echo-circuit recited

in claim 14. Since the references do not disclose or suggest all elements of amended claim 14, claim 14 is allowable.

Claims 15-20 are allowable at least because they depend from allowable claim 14 and for the additional features they recite. Withdrawal of the rejection of claims 1-7, 9, and 11-20 under 35 U.S.C. §103 (a) is respectfully requested.

In view of the above remarks, Applicants respectfully submit that the application is in condition for allowance. Prompt examination and allowance are respectfully requested.

Should the Examiner believe that anything further is desired in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

Date: **January 27, 2005**

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